REMARKS

The Office Action of December 18, 2003 has been received and its contents carefully considered.

Claims 1-22 are pending in this application. Claims 1, 4, 6-11, 13 and 15-22 are amended herein. The independent claims are claims 1, 17 and 20.

In the Office Action, claims 1-22 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly pointed out and distinctly claim the subject matter which the applicant regards as the invention. Specifically, the Examiner points to each of claim sets 1-16, 17-19, and 20-22 as being directed to an apparatus, and asserts that the essential cooperative relationships between structural elements in the claims have been omitted, such omission amounting to a gap between the necessary structural connections (citing MPEP §2172.01).

In response, claims 1, 4, 6-11, 13 and 15-22, and particularly independent claims 1, 17 and 20 are amended herein to more fully define the connections between the elements comprising the apparatus to which each claim set is directed. Accordingly, the Examiner is respectfully requested to enter the amended claims and withdraw the §112 rejection.

The applicant notes with appreciation the Examiner's early indication that claims 17-22 would be allowable if rewritten or amended to overcome the rejection under 35 USC §112, second paragraph, set forth in the Office Action. As noted immediately above, claims 17-22 are amended herein to overcome the §112 rejection. Therefore, allowance of amended claims 17-22 is appropriate.

The applicant further notes with appreciation the Examiner's indication that claims 3-16 would be allowable if rewritten to overcome the rejection under 35 USC §112, second paragraph, set forth in the Office Action, and also to include all of the limitations of the base claim and any intervening claims.

Claims 1 and 2 stand rejected under 35 U.S.C. 103(a) as being obvious over the acknowledged prior art in view of Lelm et al. (U.S. Patent No. 5,448,715). It is respectfully submitted that for at least the following reasons, the amended claims patentably distinguish over the applied prior art.

In the Office Action, the Examiner points to the acknowledged prior art (PA), page 2, line 1 to page 3, line 8, of the originally filed specification, as disclosing the claimed invention

including an interrupt setting pulse generating section, a register, an interrupt clearing pulse generating system, and an interrupt signal processing apparatus readable as a "control circuit." The Examiner acknowledges, however, that the PA fails to disclose the use of a "first synchronization unit," "second synchronization section," and a "delay circuit." To cure this acknowledged deficiency in the PA, the Examiner asserts that Lelm discloses a dual clock domain interface for synchronizing data (including interrupt signal) from one device operated at a first clock, to another device operating at a second clock; wherein data is synchronized with either the first or the second operating clock depending on the type of data transfer (see at least Figure 2 and description thereof); and wherein the first clock is different from the second clock; and a clock control circuit (214) is readable as a "delay circuit." The Examiner argues that it would have been obvious to one of ordinary skill in the art at the time the invention was made to synchronize the interrupt signals of the PA using the techniques taught by Lelm for the purpose of allowing interrupts to be processed with a higher clock rate in one device without being constrained by a slower clock speed in another device.

In applying the Lelm reference, the Examiner asserts that the clock control circuit shown in Figure 2 is readable as a "delay circuit." The Applicant respectfully disagrees. Lelm is directed to a Dual Clock Domain Interface, which allows a CPU, for example, operating at one clock speed to interface with a memory bus, for example, operating at a second clock speed (see Abstract). In Lelm, a domain translation buffer 216 (see Figure 2) takes a signal from one clock domain and "translates" it into another clock domain. The signal translation is accomplished using special clock signals (defined for each domain) which depend upon the direction a signal is propagating. Such domain translation clocks 212a, 212b are generated by the clock control circuit 214 (see column 5, line 65 through column 6, line 5). In short, the function of Lelm's clock control circuit is to generate clock signals. Nothing in Lelm teaches or suggests that the clock control circuit can be read as a "a delay circuit connected between said register and said first and second synchronization sections, to provide, while said one pulse signal is being input to said register, a time delay to operations of said synchronization section being operated in synchronization with said clock on which said pulse generating section used to generate said other pulse signal is operated, in order to prevent duplicated inputting of both said pulse signals to the register" (emphasis added), as claim 1

requires. The purpose and function of the clock control circuit in Lelm and the delay circuit in the present invention are clearly very different.

As noted above, the Examiner also acknowledges that the PA does not disclose the use of a "first synchronization section" or a "second synchronization section," to which the delay circuit is to be connected. However, the Examiner does not even attempt to point out or suggest in the Office Action what elements in Lelm correspond in configuration or function to the synchronization sections of the claimed invention.

As also noted earlier, the Examiner suggests, in a parenthetical, that that Lelm discloses a dual clock domain interface for synchronizing interrupt signals. What Lelm discloses, with reference to Figure 1, is that bus memory 108 signals fall into three different categories: 1) protocol, 2) interrupt and reset, and 3) data. Lelm indicates that the majority of communication between a CPU 102 and memory 110 on bus 108 are protocol signals. Interrupt signals (not shown) include both external and dedicated synchronous machine check lines (column 5, lines 35-45). Lelm does not discuss in any further detail the handling of interrupt signals, nor does it suggest in any way the techniques used in the present invention for doing so.

Thus, the Examiner has not met the burden of providing a basis in fact and/or cogent technical reasoning to support the conclusion that one having ordinary skill in the art would have been motivated to combine the references to arrive the claimed invention. For at least the foregoing reasons, it is respectfully submitted that amended claim 1 patentably distinguishes over the applied combination of the acknowledged prior art and Lelm. Further, claims 2-16 distinguish over the applied prior art for at least the reason that they depend from claim 1.

In summary, it is respectfully submitted that the application, as now amended, is in condition for allowance, and a notice to that effect is earnestly solicited.

[Continued on next page]

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange such an interview.

Respectfully submitted,

May 18, 2004
Date

Phillip G. Avruch - Reg. No. 46,076
RABIN & BERDO, P.C.
Telephone: 202-371-8976
Telefax: 202-408-0924
CUSTOMER NO. 23995

PGA/